REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of June 5, 2003 (hereinafter "Office Action"). Applicants especially appreciate the indication that Claims 6 and 16 recite patentable subject matter. In response, Applicants have amended Claim 1 to include the recitations of Claims 2, 5, and 6, which have been canceled without prejudice or disclaimer. Claim 3 has been amended to correct its dependency in light of the cancellation of Claim 2. In addition, Claims 20 - 28, 30, and 31 have been canceled without prejudice or disclaimer. Accordingly, the sole remaining issue for consideration is the patentability of Claims 11 - 19 and 29.

Applicants respectfully submit that the cited references fail to disclose or suggest all of the recitations of independent Claims 11 and 29. Therefore, Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 11 and 29 are Patentable

Independent Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art ("Admission") in view of U. S. Patent No. 5,946,712 to Lu *et al.* (hereinafter "Lu"). Independent Claim 29 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Admission in view of Lu and further in view of Japanese Publication No. JP 01161912 to Yoshimori (hereinafter "Yoshimori"). Independent Claim 11 is directed to an integrated circuit device that comprises a delay circuit that is described as follows:

> a delay circuit that is configured to receive an input data signal in response to a clock signal and is further configured to generate an output data signal by delaying the input data signal;...

Similarly, independent Claim 29 is directed to a method of operating an integrated circuit device and includes the following recitations:

> storing delay information in a memory unit;
> receiving an input data signal in response to a clock signal;
> delaying the input data signal based on the delay information to generate an output data signal; and
> receiving the output data signal at a plurality of devices in response to

the clock signal.

In rejecting Claims 11 and 29, the Office Action cites FIGS. 3 and 5 of Lu as disclosing a delay circuit that is configured to delay a clock signal. (Office Action, pages 3 and 4). Applicants acknowledge that Lu discloses a programmable delay module 160 that is configured to delay an input clock signal 180. Applicants submit, however, that Lu contains no disclosure or suggestion of delaying an input data signal as recited in Claims 11 and 29.

Moreover, Applicants submit that Yoshimori fails to provide the teachings missing from Lu. As shown in FIGS. 3 and 6 of Yoshimori, input buffers 4 receive a master clock from a master clock input buffer 3. The master clock is delayed based on the contents of the shift registers 5, 61. Yoshimori appears to contain no disclosure or suggestion of delaying an input data signal as recited in Claims 11 and 29.

The Office Action does not appear to cite any specific prior art reference as disclosing or suggesting delaying an input data signal as recited in Claims 11 and 29. If the rejection of Claims 11 and 29 is maintained, then Applicants respectfully request that the rejection not be made final and that the Examiner cite to specific portions of the prior art references that are alleged to disclose or suggest the recitations of Claims 11 and 29.

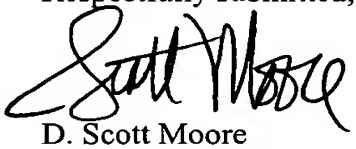
For at least the foregoing reasons, Applicant respectfully submits that independent Claims 11 and 29 are patentable over the cited references, and that dependent Claims 12 - 20 are patentable at least by virtue of their depending from an allowable claim.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

It is not believed that an extension of time and/or additional fee(s)-including fees for net addition of claims-are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper are hereby authorized to be charged to our Deposit Account No. 50-0220.

Respectfully submitted,



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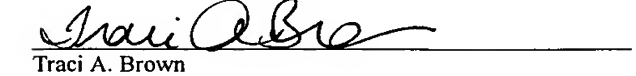
CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 4, 2003.



Traci A. Brown